

FIG. 1 (a)

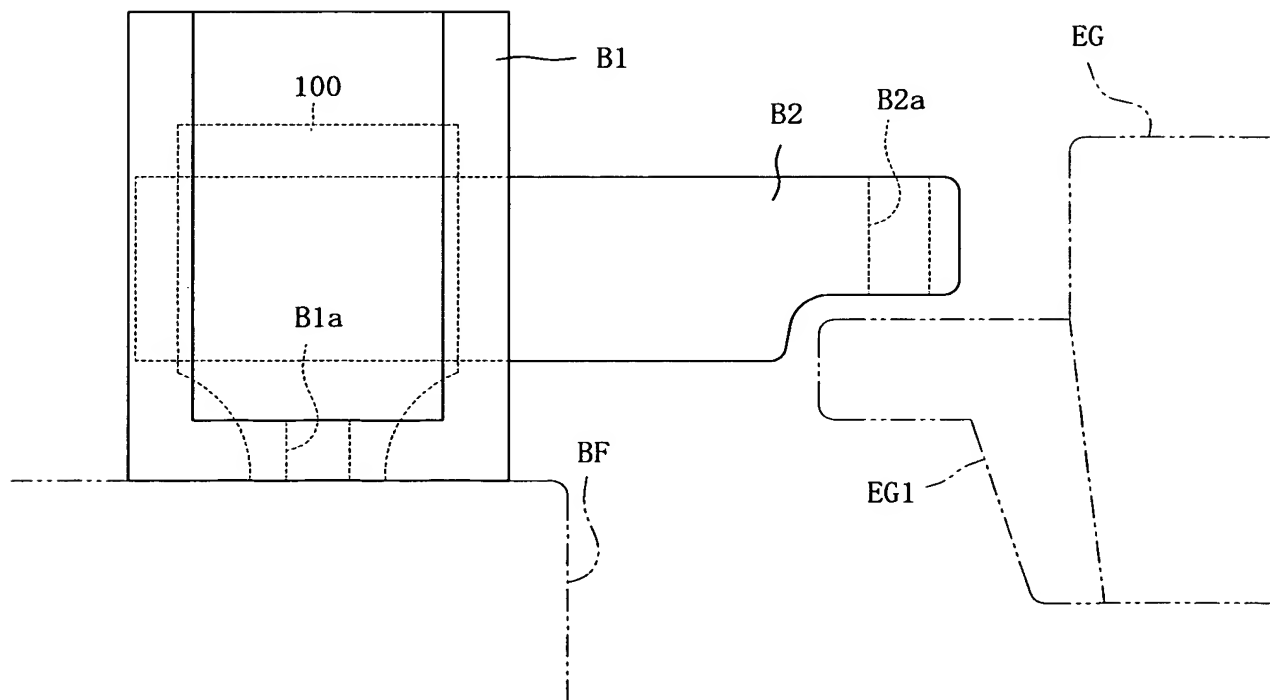
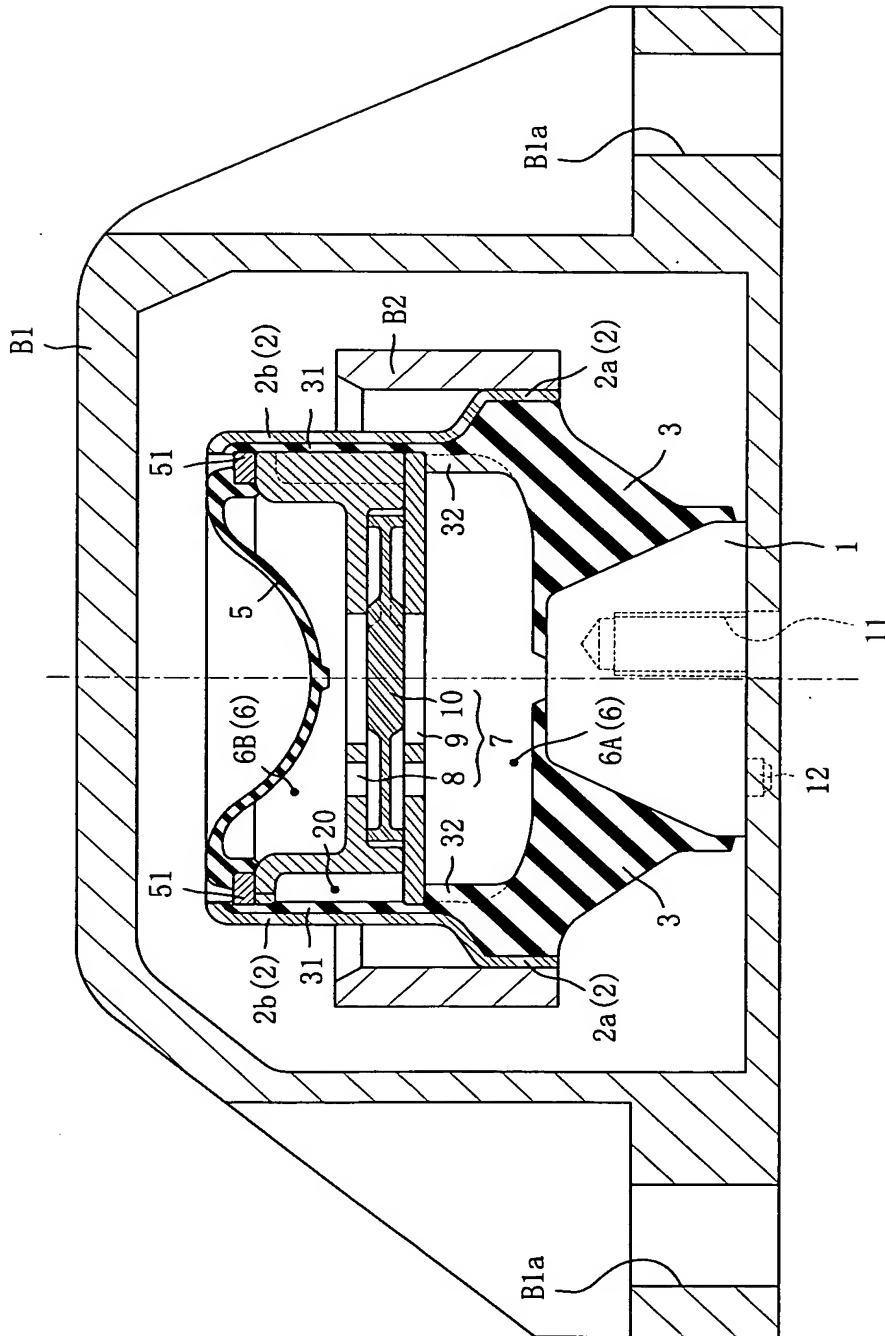


FIG. 1 (b)

FIG. 2



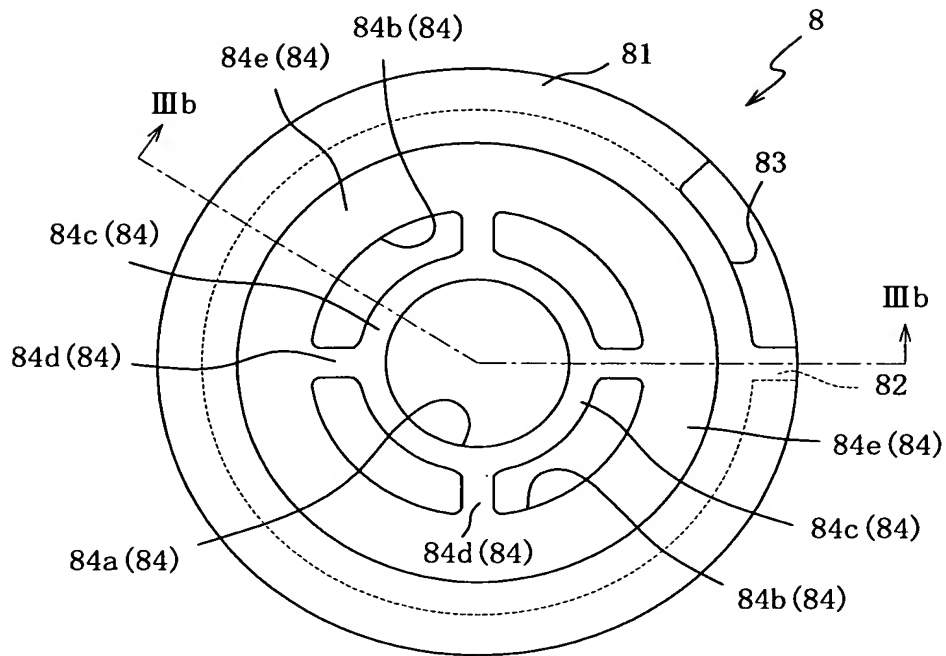


FIG. 3(a)

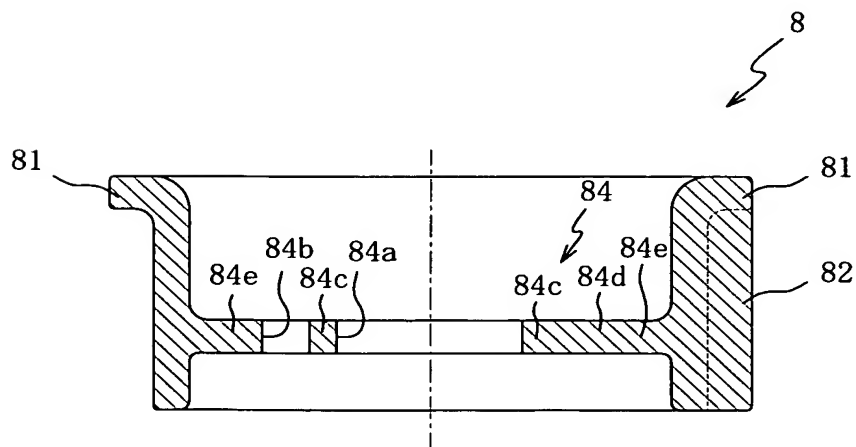


FIG. 3(b)

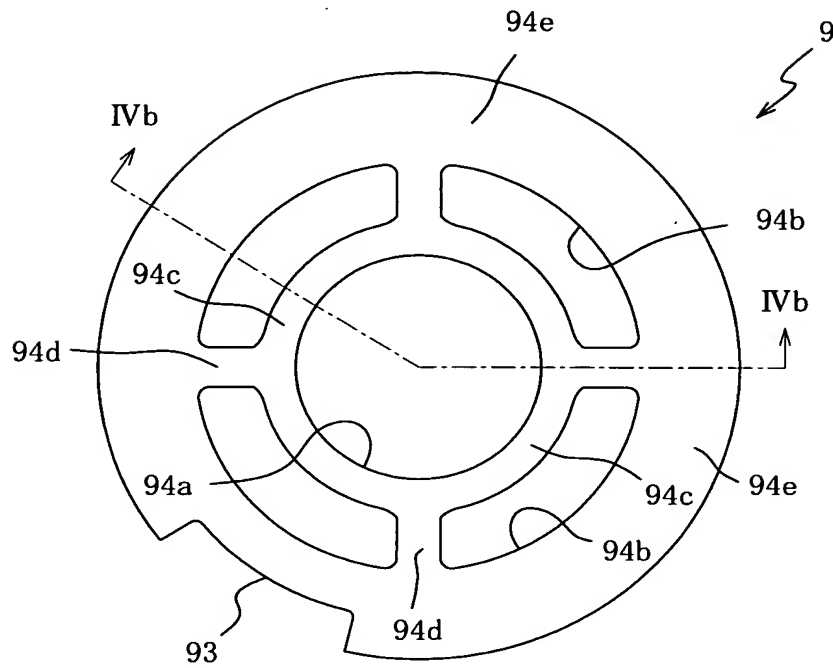


FIG. 4(a)

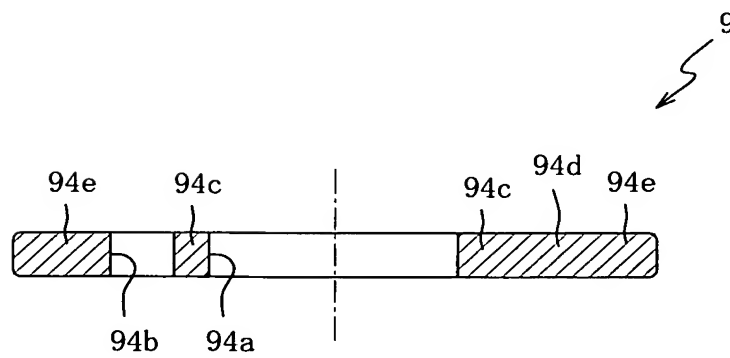


FIG. 4(b)

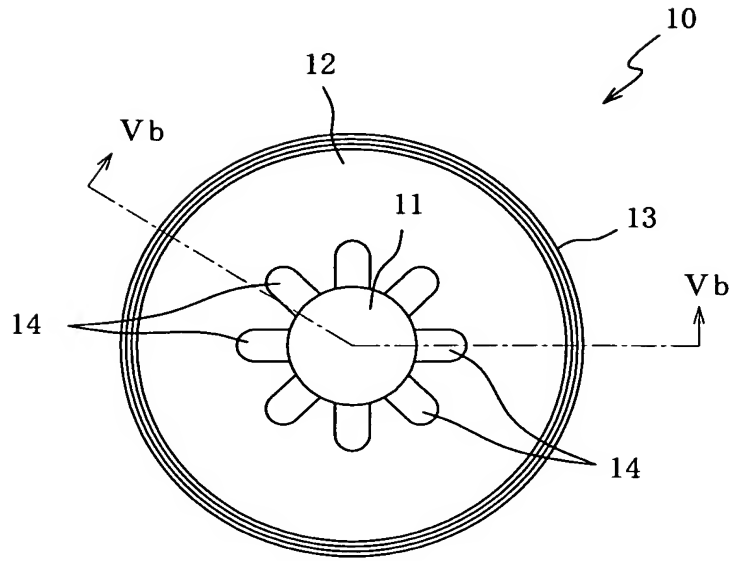


FIG. 5(a)

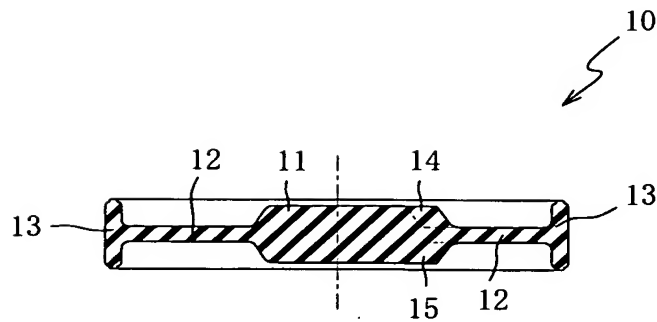
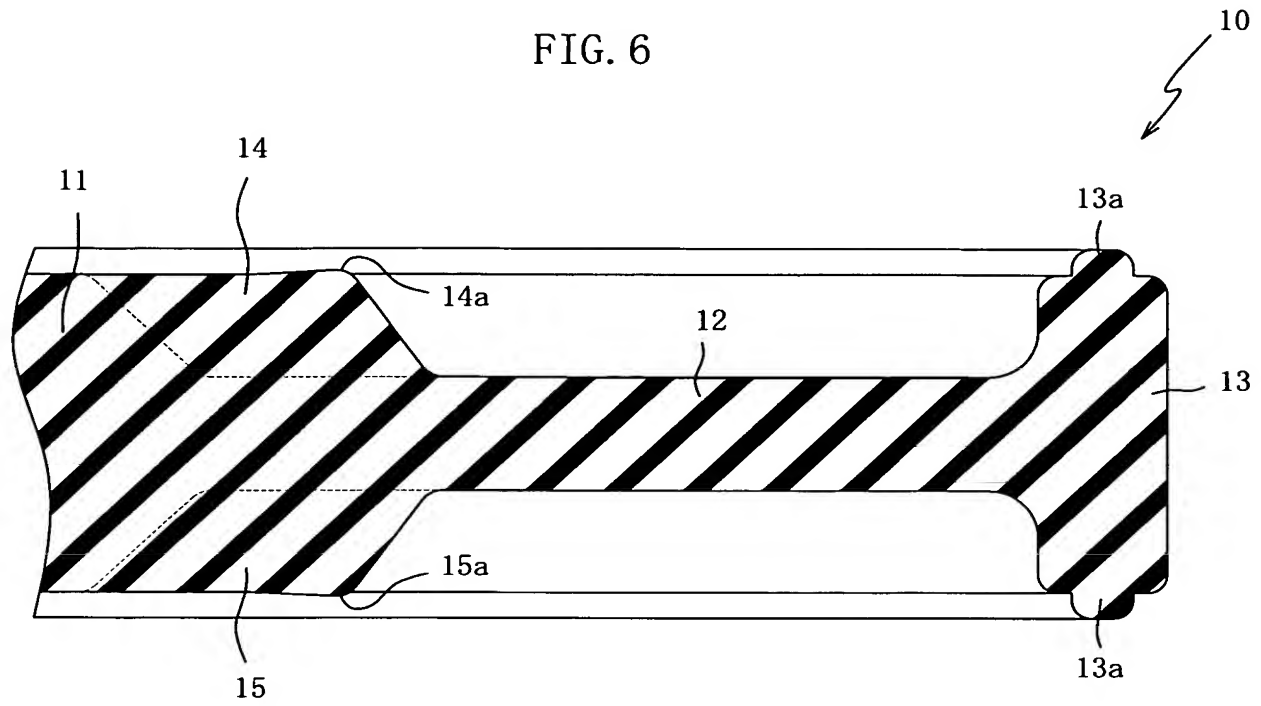


FIG. 5(b)

FIG. 6



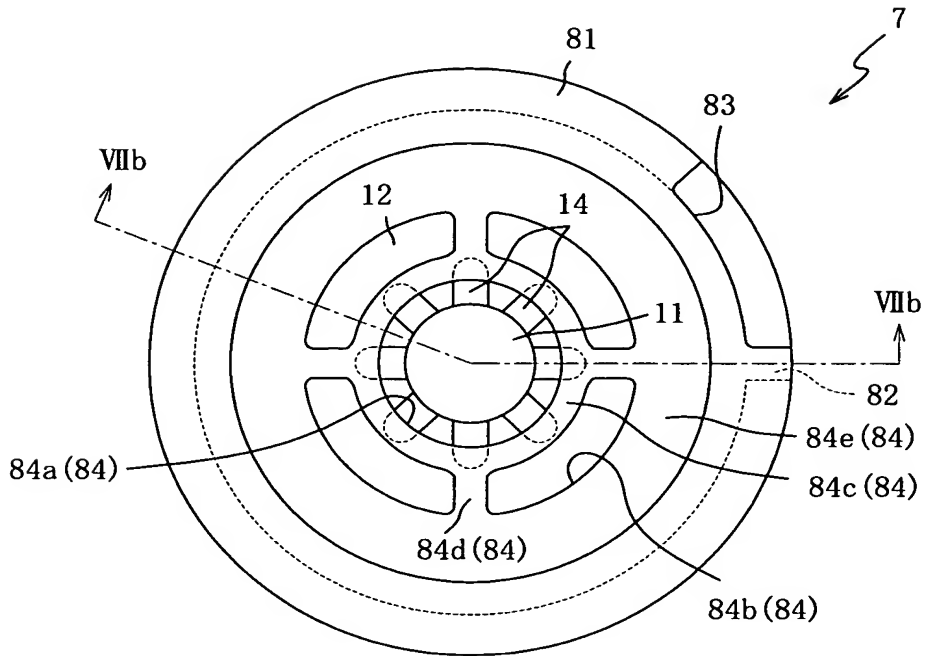


FIG. 7 (a)

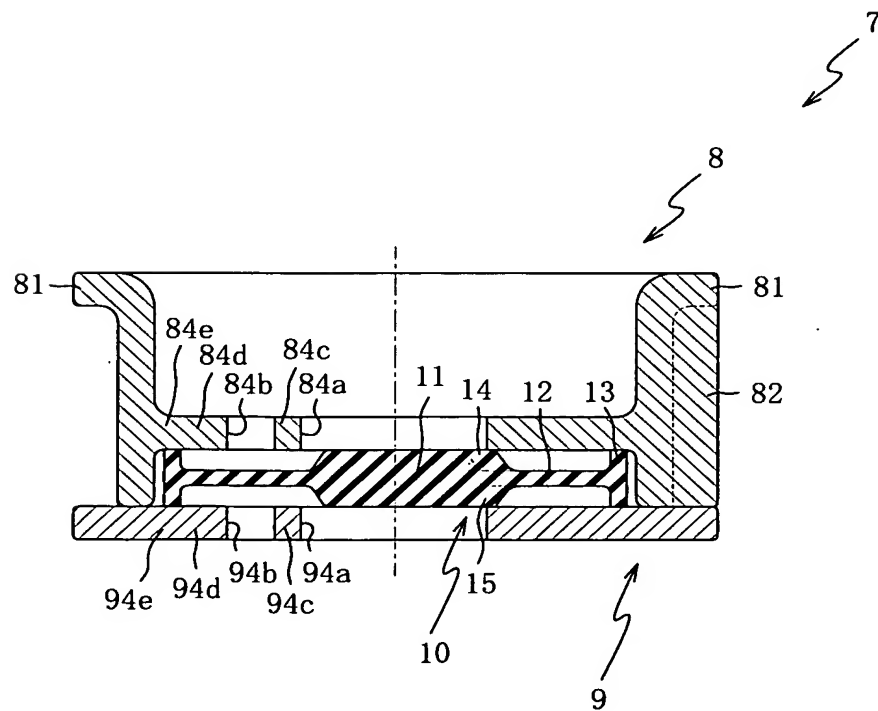


FIG. 7 (b)

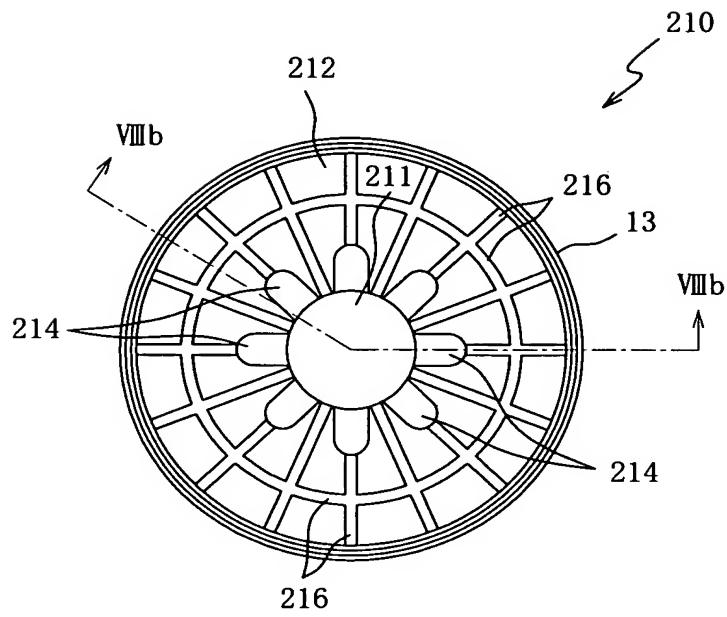


FIG. 8(a)

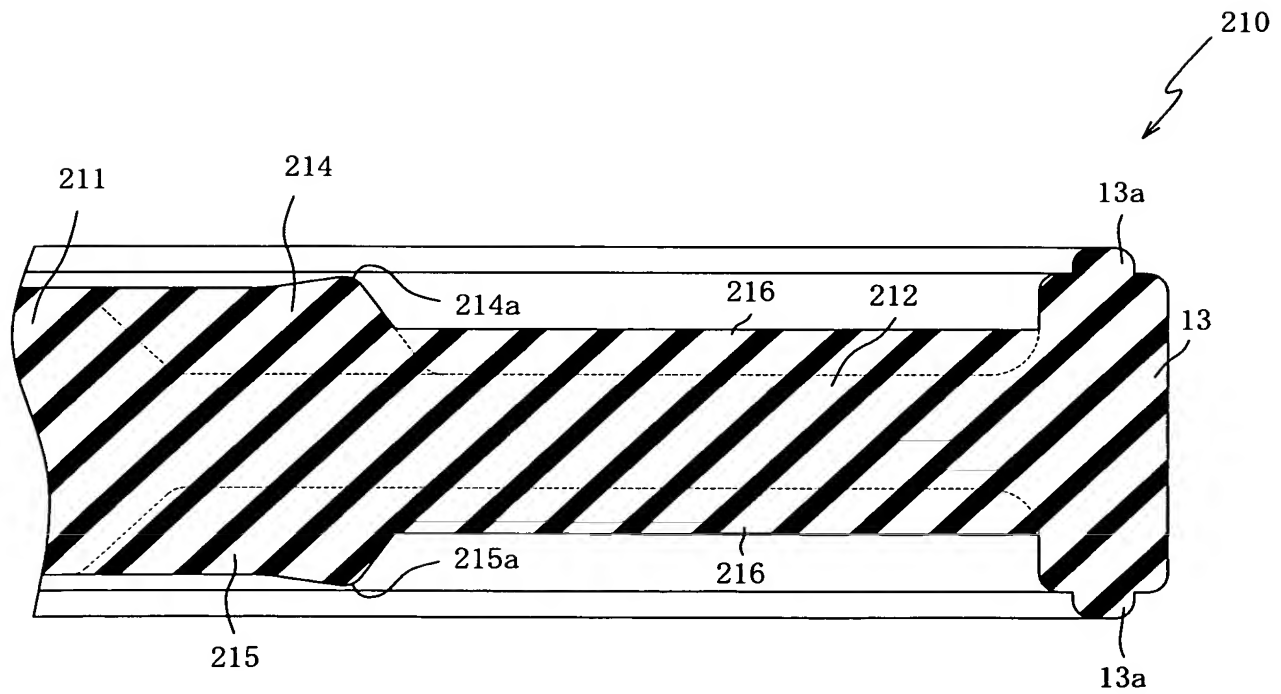


FIG. 8(b)



A detailed cross-sectional diagram of a semiconductor device along a vertical plane. The device features a central channel region (7) defined by a gate stack (8, 9, 10). This channel is flanked by source/drain regions (6A(6), 6B(6)) which are covered by a protective layer (5). The entire structure is embedded within a substrate (12) containing a trench (11). Various other components are labeled, including B1a, B12, B12b, 2a(2), 2b(2), 3, 31, 32, and 51.